CLAIMS

What is claimed is:

1. An apparatus comprising:

a physical register file in which data associated with instructions of a computer program are stored in an order that is independent of whether a processor executing the instructions is in a multithread (MT) mode or a single-thread (ST) mode.

2. The apparatus of claim 1 further comprising at least one register allocation table (RAT) to indicate allocation of the data from logical registers to physical registers within the physical register file.

3. The apparatus of claim 1 further comprising a list of physical registers within the physical register file that are not allocated to a logical register, entries in the list being completely allocated to a first thread while the processor is in ST mode and entries in the list being partitioned such that a first portion of the entries are allocated to a first thread and a second portion of the entries are allocated to a second thread while the processor is in MT mode.

4. The apparatus of claim 3 wherein a first portion of all of the physical registers in the physical register file are allocated to the first thread

and a second portion of all of the physical registers in the physical register file are allocated to the second thread if the processor is in ST mode, the first portion of all of the physical registers being larger than the second portion of all of the physical registers.

5. The apparatus of claim 4 wherein the second thread is dormant if the processor is in ST mode.

6. The apparatus of claim 4 wherein the first portion of all of the physical registers within the physical register file remain allocated to the first thread after the processor transitions to MT mode until instructions associated with data within the first portion of all of the physical registers within the physical register file are retired.

7. The apparatus of claim 6 wherein the physical registers associated with the retired instructions are indicated within the list of physical registers.

8. An apparatus comprising:

a first means for indicating registers within a physical register file for use by a microprocessor that are not allocated to logical registers, the first means being partitioned during a second mode of operation of the microprocessor and not being

partitioned during a first mode of operation of the microprocessor;

a second means for allocating the logical registers to the physical registers.

9. The apparatus of claim 8 wherein the logical registers are allocated to the physical registers independently of the relative position of the logical registers to each other.

10. The apparatus of claim 9 wherein the second means comprises a register allocation table to indicate the allocation of the logical registers to the physical registers.

11. The apparatus of claim 9 wherein the second means comprises a plurality of register allocation tables to indicate the allocation of the logical registers to the physical registers, each of the plurality of register allocation tables being associated with a separate thread of instructions.

12. The apparatus of claim 11 wherein the first mode of operation is a single thread mode and the second mode is a multiple-thread mode.

13. The apparatus of claim 12 wherein the first means is a register file comprising a list of the physical registers that are not allocated to

the logical registers.

14. The apparatus of claim 13 wherein the sum of the number of physical registers in the list and the number of logical registers associated with a single thread equals the number of physical registers within the physical register file.

15. The apparatus of claim 14 wherein a first physical register is indicated in the list after an instruction associated with data stored in the first physical register is retired.

16. A system comprising:

a memory unit to store a first and second thread of instructions;

a processor to perform the first and second thread of instructions, the processor comprising a physical register file wherein data corresponding to the first and second thread of instructions are stored in an order independent of whether the processor is in a multithread (MT) mode or a single-thread (ST) mode.

17. The system of claim 16 wherein the processor further comprises at least one register allocation table (RAT) to indicate allocation of the data from logical registers to physical registers within the physical

register file.

18. The system of claim 16 further comprising a list of physical registers not allocated to a logical register, entries in the list being completely allocated to the first thread while the processor is in ST mode and entries in the list being partitioned such that a first portion of the entries are allocated to the first thread and a second portion of the entries are allocated to the second thread while the processor is in MT mode.

19. The system of claim 18 wherein a first portion of all of the physical registers in the physical register file are allocated to the first thread and a second portion of all of the physical registers in the physical register file are allocated to the second thread if the processor is in ST mode, the first portion of all of the physical registers being larger than the second portion of all of the physical registers.

20. The system of claim 19 wherein the second thread is dormant if the processor is in ST mode.

21. The system of claim 19 wherein the first portion of all of the physical registers within the physical register file remain allocated to the first thread after the processor transitions to MT mode until

instructions associated with data within the first portion of all of the physical registers within the physical register file are retired.

22. The system of claim 21 wherein the physical registers associated with the retired instructions are indicated within the list of physical registers.

23. A method comprising:

initializing a register allocation table (RAT) to map a first group of logical registers to a second group of physical registers;

dividing a freelist of registers in half if a processor associated with the free list is in multi-thread (MT) mode;

undividing the freelist of registers if the processor is in single-thread (ST) mode.

24. The method of claim 23 further comprising transitioning from ST mode to MT mode, the second group of physical registers being interspersed throughout a physical register file.

25. The method of claim 24 wherein the second group of physical registers remain interspersed throughout the physical register file after the transition from ST to MT mode.

26. The method of claim 23 further comprising transitioning from MT mode to ST mode, the second group of physical registers being interspersed throughout a physical register file.

27. The method of claim 26 wherein the second group of physical registers remain interspersed throughout the physical register file after the transition from MT to ST mode.

28. The method of 23 wherein the logical registers are allocated to the physical registers independently of the relative position of the logical registers to each other.

29. The method of claim 28 wherein the sum of the entries in the freelist and the number of logical registers associated with a single thread equals the number of physical registers within the physical register file.

30. The method of claim 29 further comprising a indicating a first physical register in the freelist after an instruction associated with data stored in the first physical register is retired.